*Tableau 1: Converting between 4-bit binary, std_logic_vector(*to*), std_logic_vector(*downto*) and « format-base-value »*

Binary	std_logic_vector(0 to 3)	format-base-value	std_logic_vector(3 to 0)	format-base-value
0001	1	4’h1	8	4’h8
0010	2	4’h2	4	4’h4
0011	3	4’h3	12	4’hc
0100	4	4’h4	2	4’h2
0101	5	4’h5	10	4’ha
0110	6	4’h6	6	4’h6
0111	7	4’h7	14	4’he
1000	8	4’h8	1	4’h1
1001	9	4’h9	9	4’h9
1010	10	4’ha	5	4’h5
1011	11	4’hb	13	4’hd
1100	12	4’hc	3	4’h3
1101	13	4’hd	11	4’hb
1110	14	4’he	7	4’h7
1111	15	4’hf	15	4’hf

std_logic_vector(0 to 3) is numbered as so and is read in Latin (left to right) . This example uses binary 1010 which read in Latin (0 to 3) is equal to decimal 10.

Tableau 2: representation of VHDL std_logic_vector(0 to 3)

bit	1	0	1	0
index	0	1	2	3

std_logic_vector(3 downto 0) is numbered as so and is read in Arabic (right to left) . This example uses binary 1010 which read in Arabic (3 to 0) is equal to decimal 5.

Tableau 3: representation of std_logic_vector(3 downto 0)

bit	1	0	1	0
index	3	2	1	0